

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: : **Hidetaka NATSUME**  
Filed: : **Concurrently herewith**  
For: : **SEMICONDUCTOR MEMORY DEVICE.....**  
Serial No. : **Concurrently herewith**

January 15, 2002

Assistant Commissioner of Patents  
Washington, D.C. 20231

**PRELIMINARY AMENDMENT**

S I R:

Prior to the issuance of an Office Action, please amend the specification and claims as follows:

**IN THE CLAIMS:**

**Please amend the following claims with the following:**

3.(Amended) A semiconductor memory device according to Claim 1, wherein:

said second electrical conductor is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection A, the gate electrode being in common to said first driver transistor; and

a first interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said third interconnection is in contact with

a contact section connected to said first interconnection A;  
a contact section connected to a drain  
region of said second driver transistor; and  
a contact section connected to a drain region of said second load transistor.

7.(Amended) A semiconductor memory device according to Claim 4, wherein:

said inlaid interconnection is disposed so as to come in contact with  
a drain region constituting a first driver transistor which is one of said pair  
of driver transistors;  
a drain region constituting a first load transistor which is one of said pair of  
load transistors and has a gate electrode formed from a first conductive film interconnection A,  
the gate electrode being in common to said first driver transistor; and  
a first conductive film interconnection B which constitutes a gate electrode  
of a second driver transistor which is the other one of the pair of driver transistors as well as a  
gate electrode of a second load transistor which is the other one of the pair of load transistors;  
and  
said second conductive film interconnection is in contact with  
a contact section to reach said first conductive film interconnection A;  
a contact section to reach a drain region of said second driver transistor; and  
a contact section to reach a drain region of said second load transistor.

13.(Amended) A semiconductor memory device according to Claim 1, wherein a refractory  
metal silicide layer is formed on the surface of every gate electrodes, source regions and drain  
regions of said pair of driver transistors, said pair of load transistors and said pair of transmission  
transistors.

17.(Amended) A method of manufacturing a semiconductor memory device according to Claim 14, wherein:

said inlaid interconnection is formed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is formed to come into contact with every one of contact sections which are made by forming, concurrently, a contact hole to reach said first conductive film interconnection A, a contact hole to reach the drain region of said second driver transistor, and a contact hole to reach the drain region of said second load transistor; and thereafter filling up these contact holes with a conductive material.

19.(Amended) A method of manufacturing a semiconductor memory device according to Claim 14, which further comprises the step of forming a refractory metal silicide layer on the surface of every source regions and drain regions of said pair of driver transistors, said pair of load transistors and said pair of transmission transistors as well as on the surface of said first conductive film interconnection which constitutes gate electrodes thereof.

**Please add the following new claims:**

20. (New) A method of manufacturing a semiconductor memory device according to Claim 16, wherein:

said inlaid interconnection is formed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is formed to come into contact with every one of contact sections which are made by forming, concurrently, a contact hole to reach said first conductive film interconnection A, a contact hole to reach the drain region of said second driver transistor, and a contact hole to reach the drain region of said second load transistor; and thereafter filling up these contact holes with a conductive material.

21. (New) A method of manufacturing a semiconductor memory device according to Claim 16, which further comprises the step of forming a refractory metal silicide layer on the surface of every source regions and drain regions of said pair of driver transistors, said pair of load transistors and said pair of transmission transistors as well as on the surface of said first conductive film interconnection which constitutes gate electrodes thereof.

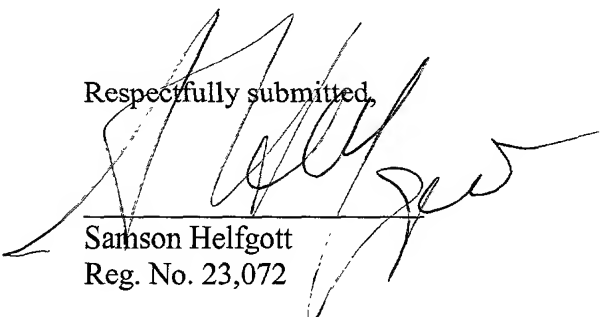
## REMARKS

This amendment is being submitted to avoid multiple dependent claims.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Favorable consideration is respectfully requested.

Respectfully submitted,

  
Samson Helfgott  
Reg. No. 23,072

Rosenman & Colin LLP  
575 Madison Avenue  
New York, NY 10022-2585  
Docket No.: NECW 19.349  
Any fee due with this paper, may be charged  
On Deposit Acct. No. 50-1290.

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**IN THE CLAIMS:**

**Please amend the following claims with the following:**

3.(Amended) A semiconductor memory device according to Claim 1 ~~or~~ 2, wherein:

said second electrical conductor is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first interconnection A, the gate electrode being in common to said first driver transistor; and

a first interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said third interconnection is in contact with

a contact section connected to said first interconnection A;

a contact section connected to a drain region of said second driver transistor; and

a contact section connected to a drain region of said second load transistor.

7.(Amended) A semiconductor memory device according to Claim 4, ~~5 or~~ 6, wherein:

said inlaid interconnection is disposed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is in contact with

a contact section to reach said first conductive film interconnection A;

a contact section to reach a drain region of said second driver transistor; and

a contact section to reach a drain region of said second load transistor.

13.(Amended) A semiconductor memory device according to ~~any one of~~ Claims 1-12, wherein a refractory metal silicide layer is formed on the surface of every gate electrodes, source regions and drain regions of said pair of driver transistors, said pair of load transistors and said pair of transmission transistors.

17.(Amended) A method of manufacturing a semiconductor memory device according to Claim 14, 15 or 16, wherein:

said inlaid interconnection is formed so as to come in contact with

a drain region constituting a first driver transistor which is one of said pair of driver transistors;

a drain region constituting a first load transistor which is one of said pair of load transistors and has a gate electrode formed from a first conductive film interconnection A, the gate electrode being in common to said first driver transistor; and

a first conductive film interconnection B which constitutes a gate electrode of a second driver transistor which is the other one of the pair of driver transistors as well as a gate electrode of a second load transistor which is the other one of the pair of load transistors; and

said second conductive film interconnection is formed to come into contact with every one of contact sections which are made by forming, concurrently, a contact hole to reach said first conductive film interconnection A, a contact hole to reach the drain region of said second

driver transistor, and a contact hole to reach the drain region of said second load transistor; and thereafter filling up these contact holes with a conductive material.

19.(Amended) A method of manufacturing a semiconductor memory device according to ~~any~~  
~~one of~~ Claims 14-18, which further comprises the step of forming a refractory metal silicide  
layer on the surface of every source regions and drain regions of said pair of driver transistors,  
said pair of load transistors and said pair of transmission transistors as well as on the surface of  
said first conductive film interconnection which constitutes gate electrodes thereof.